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(to be used for all correspondence after initial filing)

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Filing Date	May 15, 2001
First Named Inventor	MOORE, Brian
Group Art Unit	2858
Examiner Name	
Total Number of Pages in This Submission: 24	Attorney Docket Number: 11157-23

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November 28, 2001

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416 957 1697 sbeney@bereskinparr.com

Your Reference: 09/854,905
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9 / Priority Doc.
E. Willis
12-3-01

By Courier

Honorable Commissioner of Patents
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Dear Sir:

Re: U.S. Patent Application Serial No. 09/854,905
Title: WIRELESS RADIO FREQUENCY TECHNIQUE DESIGN AND METHOD FOR TESTING OF INTEGRATED CIRCUITS AND WAFERS
Filed: May 15, 2001
Inventor: MOORE, Brian

To satisfy the requirement of 37 U.S.C. Section 1.55 (2), the Applicant hereby submits a certified copy of the foreign patent application from which priority was claimed for the above-referenced U.S. patent application.

Yours truly,

Stephen M. Beney/TO
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Encl.

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Canadian Patent Office

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This is to certify that the documents attached hereto and identified below are true copies of the documents on file in the Patent Office.

Specification and Drawings, as originally filed, with Application for Patent Serial No: **2,308,820** on May 15, 2000, by **THE GOVERNORS OF THE UNIVERSITY OF ALBERTA,** assignee of Brian H. Moore, for "Wireless Radio Frequency Technique Design and Method for Testing of Integrated Circuits and Wafers".

Agent certificateur/Certifying Officer

November 16, 2001

Date

Canada

(CIPO 68)
01-12-00

OPIC CIPO

Abstract

A wireless technique for testing of Very Large Scale ICs and wafers is presented. Presented is a test technique that uses standard CMOS without the use of inductors to achieve wireless parametric testing. In terms of existing technologies this system has virtually no area overhead, minimal power requirements and no process or design changes are required. A major feature is that wafer contact is not required. This work shows that a considerable reduction in testing time is possible with this technique. Also presented are specific circuits and simulations showing characteristics of operation under varying conditions. The circuit operation is shown to work down to a 1 volt and sub milliwatt power level at the same time as being $1/10000^{th}$ the area of a Pentium class VLSI circuit.

Wireless Radio Frequency Technique Design and Method for Testing of Integrated Circuits and Wafers

I Introduction

As VLSI technology approaches 1 volt or sub-volt operating levels new possibilities and new applications arise which were not possible in older technology. This wireless system is an example of a new approach. The increasing density and complexity of VLSI circuits has led to a problem of visibility and accessibility in the production and testing of such devices. At the same time as increasing density and complexity of circuits the number of input/output pins remains relatively constant or even limited by geometric constraints. The opportunity for a wireless methodology for testing is evident. In this paper we present a method to access parametric information of circuits operating at full speed on wafer. To be useful, the technique must span a range of technologies and feature sizes as well as be robust over a widely varying power supply. The contradiction of increasing importance and decreasing access leads to manufacturing uncertainty, which leads to increased cost. Increasing wafer sizes with decreasing feature size, coupled with more complex manufacturing processes, cause testing to be a critical element in VLSI manufacturing. The internal circuits in VLSI circuits are getting less accessible as the complexity grows in both fabrication technique and design finesse. It is no longer the case that the characteristics of the devices are measurable or even accessible using existing methods of testing. The SIA 1999 Roadmap [1] suggests that the cost of a transistor will equal the cost of its testing by 2015 if improvements and innovation are not made to testing VLSI circuits. The number of devices per wafer has increased and the need for testing has not abated with newer fabrication techniques. Testing using the existing techniques of on chip or on wafer probing is an

expensive and time-consuming process. As feature sizes decrease, the need of added testing pads and increased placement precision of testing probes is more and more demanding and costly.

In addition to giving important results the proposed testing approach can be carried out much earlier in the manufacturing value chain. Information about IC parameters, if obtained earlier in the manufacturing chain, can lead to feedback in the production process. Both the feedback for quality control and feedback for process control adjustment are important in modern manufacturing of integrated circuits. The ability to cull bad or out of spec circuits or wafer areas before wafer probe test and packaging is a large economic advantage. The authors present the overall Wireless Test technique and schema for implementations. Presented also are VLSI circuit designs and layouts for specific on wafer test circuits. Simulation results for these circuits are also presented. The technique can be applied to a range of technologies from 1 micron, two metal CMOS to state of the art, .18 micron, five metal advanced low voltage CMOS. Other technologies such as SiGe or GaAs could potentially use this technique as well. The enabling technologies for this are a combination of very low power and voltage design techniques, sub micron circuit topologies and characteristics, high-speed digital and analog design, physical characteristics and knowledge of wireless modulation and detection methods. These techniques are combined in the design. An overriding goal is the use of standard processes without process or design rule violations.

II Background

Why would anyone wish to do on-wafer testing for IC parameters? The answer is simple economics. Better and earlier testing techniques will reduce costs by discovering faults before the expense of dicing and packages occurs. This is especially true for systematic faults such as bad metal deposition. Also, costs can be reduced by earlier detection and remediation of

process problems, thereby improving the process before valuable chips are lost through process errors. Another reason for parametric testing is that fact that at very high speeds and small dimensions, VLSI circuits operate at the edge of analog behavior, where digital testing techniques are of insufficient benefit.

The basis of the wireless wafer tester are an off-chip tester and a test circuit on the wafer that receives a signal, modifies it, and transmits that modified signal back. The off wafer circuit is needed for sending the initial signal and receiving the altered one. The main limit of this concept is the test chip itself, as the off-chip tester can be as complex as needed, without affecting the test itself. The test chip, however, is limited because of economic considerations in size. The test chip is also limited by technology in its ability to operate at reduced power and voltage.

The implementation of our design must include some type of interface circuitry for input and output. It must also include control circuitry and characterization circuits. All of this must be done with minimal power, voltage, and size. The power and voltage must be kept low as there is no power source other than the incident energy from the signal sent. The size must be minimized to reduce the overhead costs associated with including these test sites on wafers. The necessary on-chip components are therefore an antenna, power and high frequency rectification, control circuitry, sensing circuitry, and a method of telemetry to send results back to the off chip test unit.

III Design

To achieve a completely non-contact form of testing particular attention must be given to antenna and coupling issues, as well as the extreme low power requirement. Several antenna configurations are possible for on wafer use. Each could

be constructed out of long metal lines on the wafer or possibly from the metal pad rings used for VDD and VSS on the individual dies surrounding the test site. These rings could be connected together, die to die, to form a patch antenna with dimensions in the centimeters. This would then allow for operation on the order of GHz as the frequency of the incident RF waveform. Fig. 1 is an illustration of test set up showing testing antenna and wafer. Several alternative configurations of antenna are possible including integral antennas on silicon dies [2].

In this design we will utilize the "antenna effect" for the generation of the power for the circuit. The "antenna effect" is typically to be avoided in VLSI processes and is the one design rule that will be compromised to achieve our goals, though perhaps only inter-chip wise. The antenna must maximize the amount of incident energy it receives, and to minimize the amount of energy needed to send the test results back to the off-chip tester.

We chose to use a voltage tripler for the rectification, to provide as large a voltage as possible given the low level of impinging RF energy. The goal is to have a test circuit which is powered up and working off a low level impinging RF energy. A power level which is below that of activation any of other circuitry on the wafer. Peripheral circuitry such as over voltage clamping is contemplated to be needed as well. There are several ways to implement such clamps such as a series of forward connected diodes or shunt transistor regulators. In the present design the diodes are constructed out of N-well FETs connected as diode. Fig 2 shows a typical voltage tripler circuit.

For control circuitry, we used a nine bit decoder, based on a shift register, which cycled through the tests by self activating enable signals one at a time. The master clock pulses are generated by the five-inverter ring oscillator and have two purposes. One purpose of the ring oscillator is to generate the

signals for the timing of the rest of the circuitry. The other purpose is to provide a clock whose timing is proportional to the parameter tested. This master clock is generated locally by the ring counter on wafer. The incident RF energy is used simply to create a local DC bus voltage (VDD - VSS) to power the ring counter and the rest of the circuitry. Of paramount importance is low power and low voltage operation. The signal from the master clock which contains in its frequency the parametric information is sent back through the antenna to an external receiver. The clock signal can modulate the antenna through several different means.

In the present design the test results are a frequency shift of the master ring oscillator which lasts for 32 clock periods per test. In this way each test lasts 32 clock periods which are received by the off wafer test receiver. A simple off wafer loop antenna can be used to localize both the energization of the test region as well as reception of the test results. For signals generated on wafer back to the test unit one coupling method is to simply transmit the signal to the antenna through a buffer. Another method is to modulate the impedance of the on wafer antenna and thereby re-radiate a modulated signal. A third method may be to heterodyne the test signals and the incoming RF energy with a non-linear element such as a diode to produce an AM or FM mixing/heterodyning and modulation and re-radiation of the incoming carrier. In this paper our results are based on a simple capacitively coupled buffer.

The nine-bit decoder used to sequence the tests is basically a dynamic shift register which shifts a one bit through the chain which is recycled at the end. This logic style is chosen for its minimal transistor count and its ability to operate a very low voltages. The dynamic power consumption is not critical as this circuit is operated at 1/32 of the master clock. Additional circuitry for master reset and startup are included in this

shifter so as to begin a clean test as fast as possible after power up.

For the master oscillator we used a ring counter made of five inverters. It is standard in CMOS designs to use the characteristics of ring oscillators for the determination and confirmation of several parametric and design variables. Typically a ring oscillator of 101, or some other large odd number of, inverters or simple gates are used. The results are commonly tabulated and used for comparison and calculations for simulations and for comparison during manufacture. These devices provide a test confirmation using probes in a typical test station. We chose a simple inverter ring as the basis of the design to allow some comparison in terms of testing times and results between our circuit and standard results. In this way it may be possible to compare gate delays or perhaps parameters such as oxide thickness during multi-variable testing such as contemplated here.

Several different types of inverters were designed, modeled, and tested via simulations to discover which were the best for low-power, high-frequency, and low-voltage operation. These included a basic CMOS inverter of two transistors, a full feedback form of the Schmitt Inverter, a partial feedback of the Schmitt Inverter, a reduced voltage swing inverter, an inverter with input clamping, and inverters with unequal pull up and pull down transistor symmetry. Schmitt inverters are commonly found in circuits for providing a hysteresis like behavior which is used to increase noise immunity. They operate by providing some positive feedback to the switching input of the inverter. See Figs 3a and 3b for schematics of the Schmitt inverters.

There are a large number of possible parameters that can be tested using this method. We chose to focus on capacitance, resistance and gate delay. Capacitance was tested by using an enable signal, in conjunction with pass transistors, to divert

the signal through two paths, each with a different capacitance to ground. The change in the frequency should be representative of the difference in capacitance. Figs. 4a,b show a simplified capacitance test circuit as well as simulated frequency shift.

For resistance, we used a similar strategy, but included the resistors in series, instead of in parallel. Several types of resistive tests could be contemplated. Tests important to manufacture operation including poly resistance, metal resistance and various resistivities which reflect doping implantation etc. These are important at various stages of IC mfg. [3] as well as fundamental device operation.

For gate delay, we used a simple structure of pass transistors, and increased the amount of delay of the ring oscillator by the selected addition of two inverters. Thus the increased delay or shift in operating frequency equals that of two inverters. Fig. 5 shows the simplified test gate delay test circuit.

Fig. 6 shows the combined test circuit for the three chosen tests.

IV Results

In simulations, the voltage tripler seemed to be more of a voltage doubler, as shown in Fig 7. This is apparently due to the requirement that the threshold voltage must be overcome for every PN junction. This effectively reduced our output voltage. It is likely that this can be overcome with the use of Schottky diodes rather than the PN junction types used in this work. In Milanovic etal [4] it is shown that it is possible to construct a Schottky diode in standard CMOS technology. However, for the present work we utilized n-well PN diodes using standard CMOS techniques.

When experimenting with a variety of oscillators, it is important for this application that they operate over a range of voltages. Several of the candidate oscillators did not operate at the design goal of 1 volt. There was also a disparity among delay times and current drain. Some inverters, while using large amounts of supply current, were also rather slow. The Schmitt Inverters were found to be poorer for our purposes than a simple inverter. They used more power, more current, and had longer delay times.

Simulations of the basic oscillators were carried out at the schematic level in .5 micron 5 volt technology, .35 micron 3.5 volt technology, .25 micron 2.5 volt technology and .18 micron 2 volt technologies. These simulations were carried out at various reduced voltage levels to cull the different oscillator types. In each case the basic CMOS inverter proved the most scaleable. Fig 11 shows technology scaling verses power supply voltage current consumption. All technologies and inverters had longer startup times in simulation as VDD was reduced. The reduced voltage swing inverter operated at very low power levels and was comparable or faster than the Schmitt inverters. However ideal it may be from a power consumption point of view the reduced swing inverter did not scale to the lower voltage levels and was rejected as a candidate for the final test circuits. Fig. 8 shows power verses delay for various candidate inverters in an oscillator circuit.

We simulated the capacitance test circuitry with 200fF and 400fF loads between one set of inverter stages. There was a distinct difference between the two frequencies exhibited by the circuit during each loading. This is as we had hoped, two frequency peaks that could easily be distinguished during simulation of the circuit. There are many types of capacitors one could construct using VLSI techniques to measure various parametric effects. Because of the large scope of possibilities we chose simple capacitance to model the circuit and confirm our

assumptions. The resistance test simulations also showed two distinct frequencies. Again, this is as we had predicted. Finally, the gate delay simulations showed discernible peaks, as well. We simulated the entire test circuitry, complete with the controlling circuitry to cycle through the tests.

Additional features of the circuit include a pulse coding of the test results for serial transmission and synchronization of the test results. The first 32 clock cycles or first test sends no signal to the off wafer test circuit. The circuit cycles through the tests in the following sequence each of which lasts 32 clock cycles.

Test auto sequence is illustrated in the following steps:

Time	Test	Output
Time1	Null signal	disabled
Time2	Test 1 Free running test signal	enabled
Time3	Test 2 Capacitance test	enabled
Time4	Test 3 x2 Capacitance test	enabled
Time5	Test 4 Resistance test	enabled
Time6	Test 5 x2 Resistance test	enabled
Time7	Test 6 Propagation delay test	enabled
Time8	Free running test signal	enabled
Time9	Null signal	disabled

Cycle back to Time 1.

One should note that both the time of the test and the frequency of the signal are changing with different parameters. The constant in the circuit is the 32 cycles for each test. Using this pulse coded method the off board test unit can synchronize and know the position in time of each test. For our purposes we simply allowed the tests to run freely and recorded the voltage generated for the tests over a period of one or two test cycles. The complete test simulation is illustrated in Fig.

9. The spectrum of the test results is a convenient visual way to represent the tests. One major argument for using the master oscillator for the tests is that there is a smooth transition without glitches between tests. Observation of the output waveform showed a smooth transition at the 32nd clock cycle of each test. If different oscillators were to be used for each test a major synchronization challenge would have to be overcome if one wanted to avoid transient outputs. The synchronization would effect both the on wafer tests as well as the off wafer test circuitry. Likely the bandwidth of the test receiver would have to be increased substantially to accommodate this lack of synchronization.

Fig. 9 is a graph of the output frequencies. In the present case we utilized a simple process of Discrete Fourier Transform (DFT) integrated over the test interval of one microsecond to resolve the results. The ability to process the test results in at this speed shows the power of this technique. This is very favorable compared to a probe test which may operate with a 101 ring oscillator operating at 100 MHz or 10 microseconds per result, not to mention probe placement time. One can observe a difficulty in resolving the resistance tests from the master signal. We believe the reason the output frequency from the resistance test is similar to the basic circuit test is that the resistance caused a bias current, effectively changing the threshold voltage, Vtp vs Vtn. This changes the switching point of the circuit. This switching point then changes the speed of operation, which appears as a frequency change of insufficient magnitude. A better resistance circuit is evidently needed. Another problem with the resistance tests is they do not scale in the same way as the other tests do with power supply voltage. This can be seen crossing of lines in the Tests verses Frequency for different VDD voltages in Fig. 10. For easy interpretation of results it would be best to have the tests all scale with power supply voltage so that an absolute voltage or current reference is not required. Scaling of tests also would simplify

any automated software interpretation of test results. In any case, a distinct signature is achieved which reflects the test results. Multivariate analysis could be used to gain an understanding of deviations during mfg. using some form of signature analysis of the test results.

The inverter circuits were simulated at several voltages, .75V, 1V, 1.5V, 2V, and 2.5V and various technologies. We observed increase in current consumption consistent with expectations. We are not seeking speed so much as power minimization with a secondary goal of speed maximization.

V Further Findings

After our initial results, some reworking was carried out on the circuits. This included redesigning the basic inverters to near their minimal transistor sizes. The original implementation used approximately three times the minimum design size for gate width so as to provide sufficient drive for the various investigated peripheral circuits, dividers, parametric tests, etc. This obviously effects power consumption as well as speed. An optimized design and layout was done to reduce the sizes of the inverters. The results were that the propagation delay increased by about 10% but the power consumption dropped by about 40% and the whole circuit worked down to 1 V VDD.

Also, we had initially used a standard form of the divide by two circuit in a chain to build a divide by 32 circuit. It is actually a standard D flip flop found in many texts and used in standard products which consists of transmission gates and inverters. We modified the D flip flop it to a T one clocked by a single input line which effectively turns this FF design in to a divide by two circuit. Later, we altered it to its minimal feature sizes, and reduced the transistor count by changing it into a dynamic form of flip-flop. Contrary to several texts on

the subject we found by doing this that the power consumption for the dynamic version dropped to half of the previous levels, plus the circuit still operated at 1V and full speed. This is basically because of reduced capacitive loading on the simpler dynamic circuit which in our case is operated continuously hereby reducing its dynamic consumption. The conclusion is that the application is a major determinant of power consumption.

The final circuit with reduced transistor sized was laid out using standard VLSI cad tools using three metal layers of a 5 layer .25um single n-well CMOS process. The final layout is shown in Fig. 12 sans antenna and protection circuitry is approximately 150 by 50 micrometers. This gives an area of 7,500 um^2 which is approximately one ten-thousandth the area of a Pentium class integrated circuit. Additional protection circuitry to prevent overvoltages is contemplated to be included in the final fabricated circuit.

VI Conclusions

We have made several observations with these circuits. Most importantly, that it is possible to build simple wireless test circuits that are small and use little power. We have found that high-speed wireless communications are possible using standard tools and standard CMOS processes. We also found that Schmitt inverters have difficulties with scaling, speed, and power consumption.

We have also found that reducing size can greatly reduce the current drain without greatly increasing the delay times. And, we show that the classical flip-flops are not optimal in terms of power consumption for our circuits.

Finally, we have demonstrated that low voltage and high speed circuits can be designed in standard CMOS technology, and

that propagation delay, resistance, and capacitance can all be tested with less than 250 transistors.

References

[1] *International Technology Roadmap for Semiconductors*, SIA 1999 Edition: Test and Test equipment. Pg. 61.

[2] Brian Floyd et al. *"Wireless Interconnection in a CMOS IC with Integrated Antennas"*, IEEE ISSCC 2000 Paper WA 19.6, page 328 Feb 2000.

[3] Dieter Schroder, *Semiconductor Material and Device Characterization*, John Wiley & Sons, 1990.

[4] Veljko Milanovic et al. "*CMOS Foundry Implementation of Schottky Diodes for RF Detection*" IEEE Transactions on Electron Devices, Volume 43 Number 12, December 1996

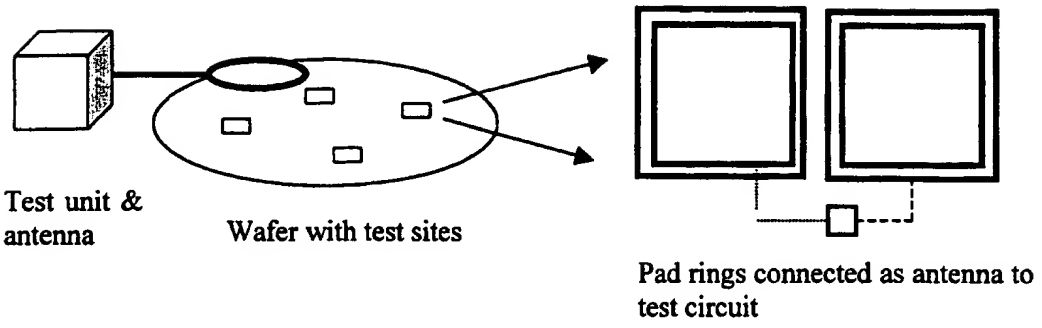

Fig. 1. Test setup

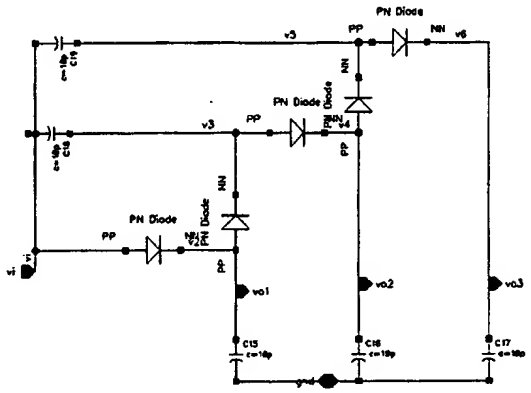

Fig. 2. Voltage tripler schematic.

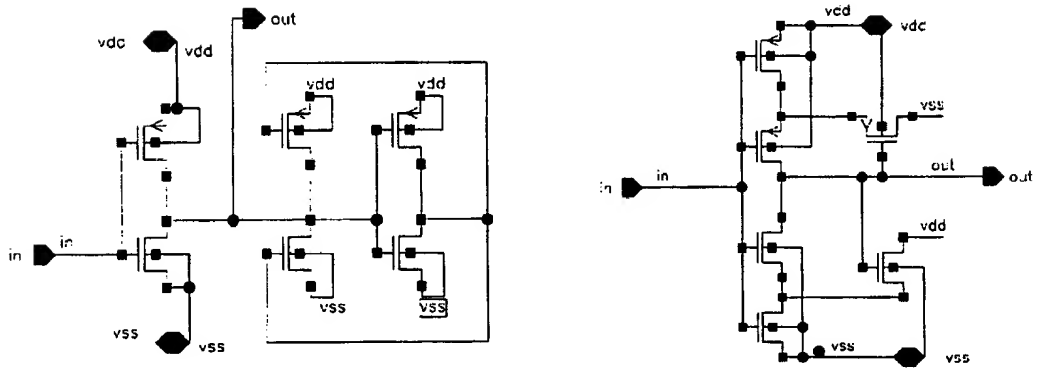

Fig 3a, b. Full feed back Schmitt and Partial feedback Schmitt inverter schematics

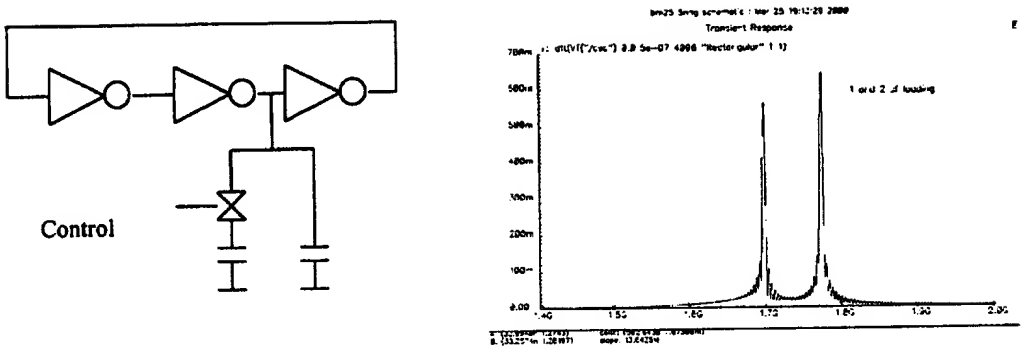

Fig. 4a, b. Capacitive schematic simplified with simulated spectral shift.

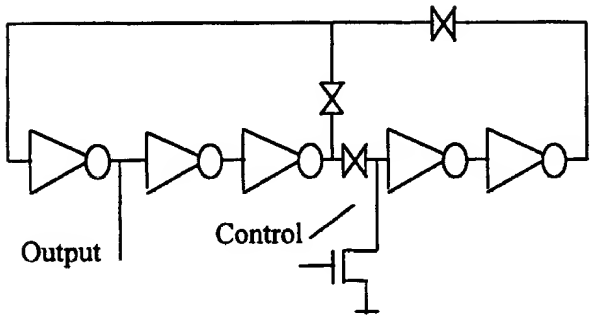

Fig. 5. Propagation delay test schematic simplified.

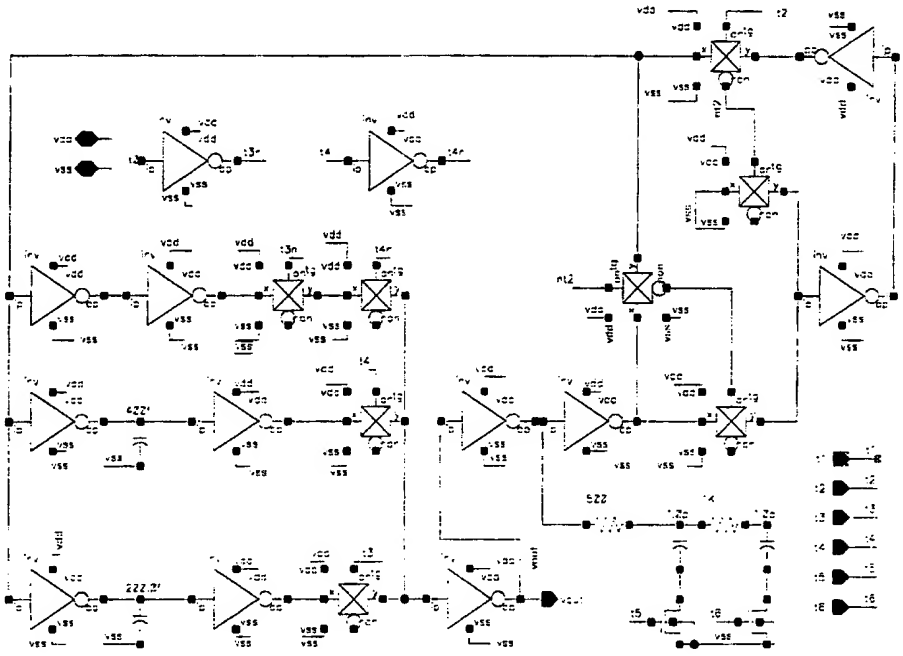

Fig 6. Schematic diagram of test oscillator circuit.

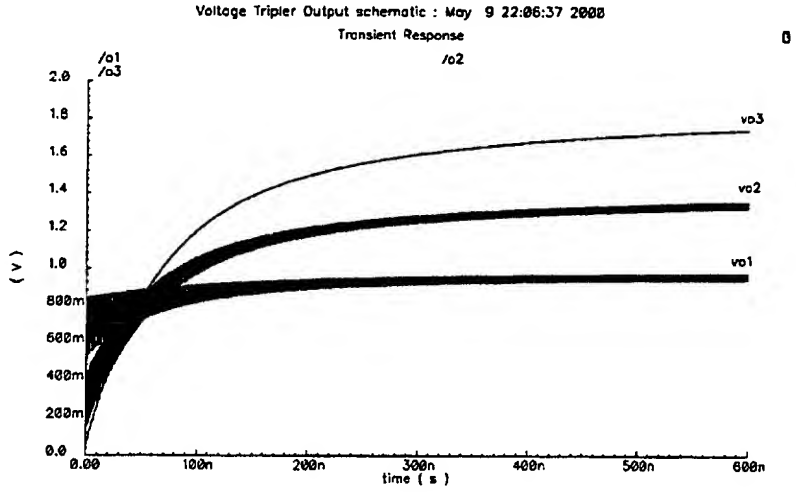

Fig. 7. Voltage tripler output.

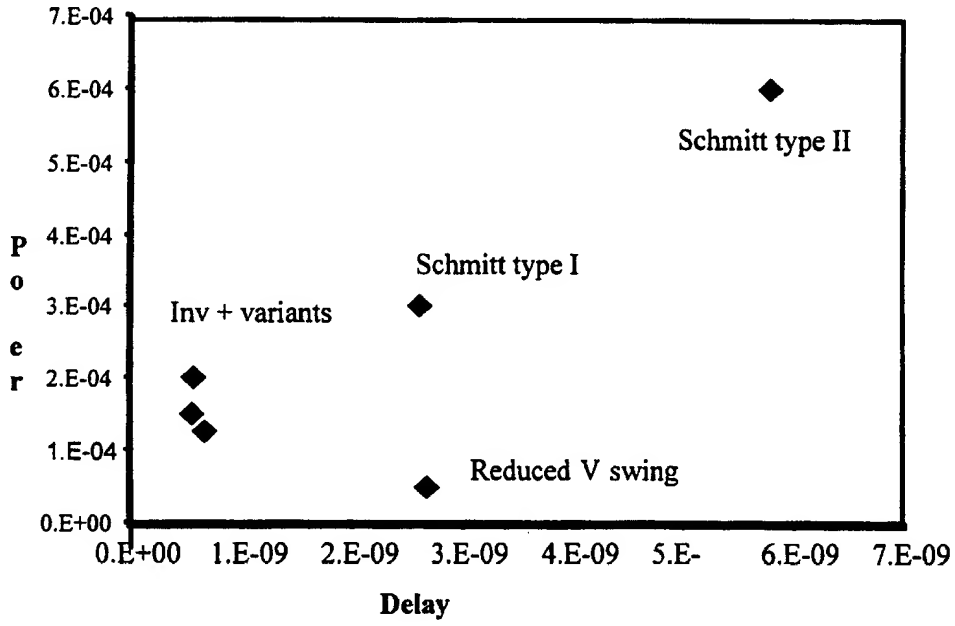

Fig. 8. Power vs. delay inverter graph.

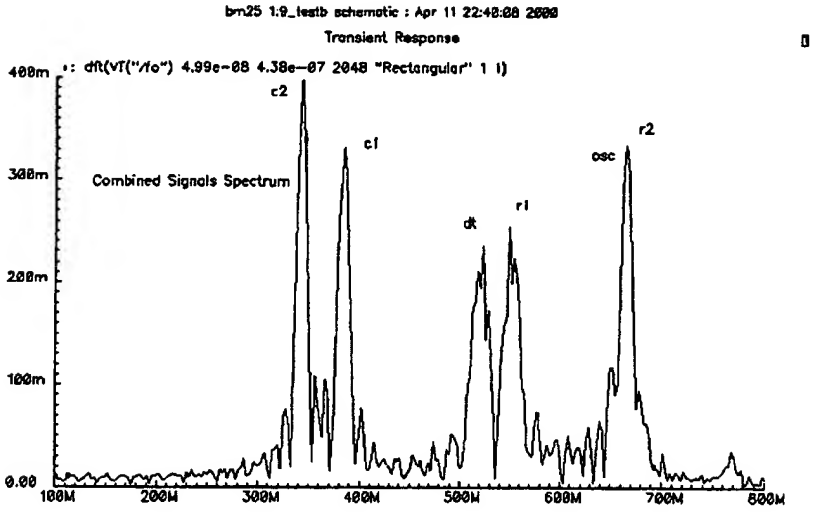

Fig. 9. Show the graph of all testing.

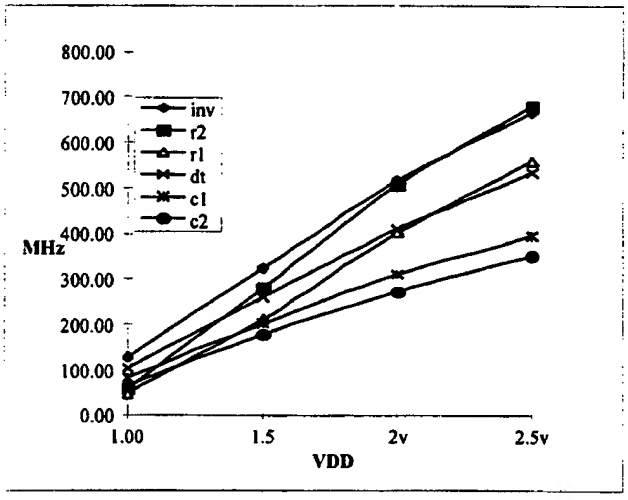

Fig 10. Scaling test results Frequency of various tests verses VDD power supply

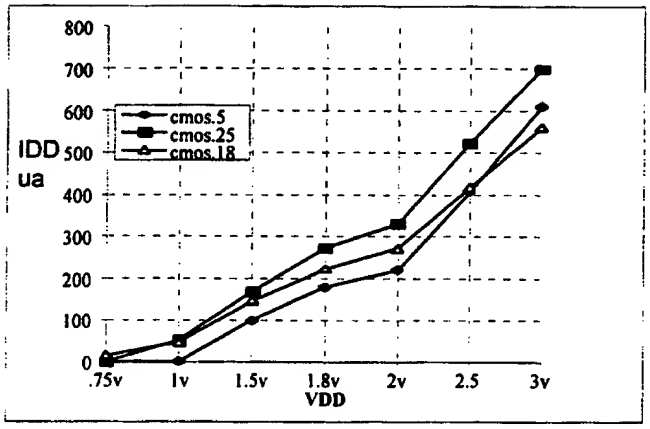

Fig. 11. Five ring oscillator current consumption verses voltage for different technologies

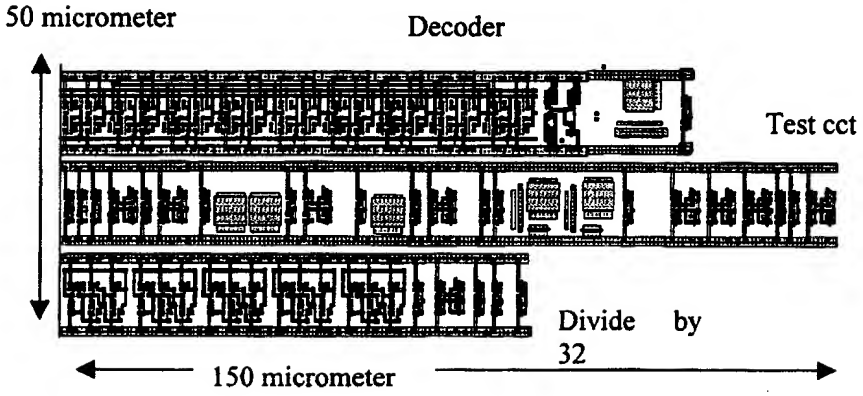

Fig 12. Design Layout using .25um 2.5volt CMOS technology.